AMENDMENTS TO THE CLAIMS

1. (previously presented) An NROM memory transistor comprising:
   a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity type than the remainder of the substrate;
   a nanolaminate, high permittivity (high-k), oxidized metal gate dielectric overlying the substrate, the gate dielectric composed of oxide-oxidized Al-oxide; and
   a control gate formed on top of the gate dielectric.

2. (original) The transistor of claim 1 wherein the gate dielectric is a composite oxide – high-k dielectric – oxide nanolaminate gate insulator wherein the high-k dielectric is a charge trapping layer formed by low temperature oxidation of metal.

3. (canceled)

4. (original) The transistor of claim 1 wherein the transistor is used in either a NOR-type flash memory structure or a NAND-type flash memory structure.

5. (original) The transistor of claim 2 wherein the charge trapping layer is comprised of a material that has a lower conduction band edge than silicon nitride.

6. (currently amended) The transistor of claim 2 wherein the gate dielectric has a larger energy barrier at a ~~between the~~ high-k dielectric ~~and the~~ - oxide ~~insulator~~ interface than at an oxide – high-k dielectric interface ~~silicon dioxide~~.

7 – 37 (canceled)

48. (canceled)